IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Hirobumi FURIHATA et al.
Title:	CONTROLLER DRIVER AND DISPLAY APPARATUS USING THE SAME
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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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Commissioner for Patents
PO Box 1450
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Sir:

The following is the Appellant's Appeal Brief under the provisions of 37 C.F.R. 41.37. This Appeal Brief is being filed together with a credit card payment form in the amount of $540.00 covering the 37 C.F.R. 41.20(b)(2) appeal fee. If this fee is deemed to be insufficient, authorization is hereby given to charge any deficiency (or credit any balance) to the undersigned deposit account 19-0741. A notice of appeal was previously on July 20, 2011.

1. Real Party in Interest

The real party in interest is Advanced Micro Devices, Inc. and Renesas, the co-assignees of this application.

2. Evidence Appendix

There are no related evidence that will directly affect, be directly affected by or have a bearing on the present appeal, that are known to appellant, the co-assignees, or the appellant's patent representative. The Evidence Appendix (Section 10), attached hereto, states "None".

3. Related Appeals and Interferences

There are no related appeals or interferences that will directly affect, be directly affected by or have a bearing on the present appeal, that are known to the Appellant, the co-assignees, or the Appellant's patent representative. The Related Proceedings Appendix (Section 11), attached hereto, states "None".

4. Status of Claims

The present appeal is directed to claims 1-3, 6-12, 19 and 20. A copy of the presently pending claims under rejection are attached herein in the Claims Appendix (Section 12). Claims 4, 5 and 18 are previously canceled, and claims 13-17, 21 and 22 are withdrawn from consideration as being directed to a non-elected invention, and thus those claims are not on appeal.

5. Status of Amendments

No amendments are being filed concurrently with this Appeal Brief.

6. Summary of the Claimed Subject Matter

Embodiments of the present invention are directed to a controller/driver used for driving display panels, particularly, to controller/drivers including display memories for storing image data (see page 1, lines 7-9 of the specification). As explained on page 16, line 25 to page 17, line 16 of the specification, image data displayed on an LCD can be partially modified through partially updating the bitmap data stored in a display memory, and the time of transmitting a "complete" bitmap data from a work memory to the display memory is reduced, thereby shortening latency from the reception of vector data by a controller/drive to the completion of the display of the associated data on the LCD. To transfer the bitmap data in a reduced duration, the work memory includes H x n data outputs for outputting pixel data associated with a line of pixels at the same time, and the display memory includes H x n data inputs for receiving the pixel data of a line of pixels at the same time.

Presently pending independent claim 1 recites:

A controller/driver comprising:

a work memory;

a graphic engine converting externally received image data into first bitmap data, and storing said first bitmap data into said work memory;

a display memory receiving and storing second bitmap data developed from said first bitmap data stored in said work memory; and

a driver circuit which receives said second bitmap data from said display memory, and drives a display panel in response to said second bitmap data received from said display memory,

wherein said first bitmap data includes a plurality of line data each including a plurality of pixel data associated with respective pixels associated with a corresponding gate line of said display panel, and

wherein said data transfer of said first bitmap data from said work memory to said display memory is performed such that each of said plurality of line data is transferred at the same time in parallel from said work memory to said display memory.

Support for a "*controller/driver*" may be found, for example, in Figures 1, 7, 8, 11, 13, 19, 24 and 25 of the drawings (see "1: Controller/Driver"), and the corresponding

description of those drawings in the specification (e.g., page 12, lines 22-27 of the specification).

Support for "*a work memory*" may be found, for example, in Figures 1, 7, 8, 11, 13, 19, 24 and 25 of the drawings (see "Work Memory 12"), and the corresponding description of those drawings in the specification (e.g., page 13, lines 1-4 and 13-14 of the specification).

Support for "*a graphic engine converting externally received image data into first bitmap data, and storing said first bitmap data into said work memory*" may be found, for example, in Figures 1, 7, 8, 11, 13, 19, 24 and 25 of the drawings (see Graphic Engine 11"), and the corresponding description of those drawings in the specification (e.g., page 13, lines 1-4 and 15-25 of the specification).

Support for "*a display memory receiving and storing second bitmap data developed from said first bitmap data stored in said work memory*" may be found, for example, in Figures 1, 7, 8, 11, 13, 19, 24 and 25 of the drawings (see "Display Memory 13"), and the corresponding description of those drawings in the specification (e.g., page 14, line 21 to page 15, line 6 of the specification).

Support for "*a driver circuit which receives said second bitmap data from said display memory, and drives a display panel in response to said second bitmap data received from said display memory*" may be found, for example, in Figures 1, 7, 8, 11, 13, 19, 24 and 25 of the drawings (see "Gate Line Driver 17"), and the corresponding description of those drawings in the specification (e.g., page 15, lines 20-24 of the specification).

Support for "*wherein said first bitmap data includes a plurality of line data each including a plurality of pixel data associated with respective pixels associated with a corresponding gate line of said display panel*" may be found, for example, on page 16, line 25 to page 17, line 9 of the specification.

Support for "*wherein said data transfer of said first bitmap data from said work memory to said display memory is performed such that each of said plurality of line data is*

transferred at the same time in parallel from said work memory to said display memory" may be found, for example, on page 17, lines 4-16 of the specification.

Dependent claim 12 recites:

The controller/driver according to claim 10, further comprising a timing controller controlling said work memory, and said display memory, and said driver circuit,

wherein said driver circuit is connected to said second bit lines, and

wherein said timing controller is adapted to deactivate said display memory to allow said first bitmap data to be transmitted from said work memory to said driver circuit through said second bit lines.

Support for "*a timing controller controlling said work memory, and said display memory, and said driver circuit*" may be found, for example, in Figures 1, 7, 8, 11, 13, 19, 24 and 25 of the drawings (see "Timing Controller 19"), and the corresponding description of those drawings in the specification (e.g., page 22, lines 13-23 of the specification).

Support for "*wherein said driver circuit is connected to said second bit lines*" may be found, for example, in Figures 1, 7, 8, 11, 13, 19, 24 and 25 of the drawings (see "Gate Line Driver 17 and LCD 3"), and the corresponding description of those drawings in the specification (e.g., page 4, lines 1-4 of the specification).

Support for "*wherein said timing controller is adapted to deactivate said display memory to allow said first bitmap data to be transmitted from said work memory to said driver circuit through said second bit lines*" may be found, for example, page 16, lines 4-24 of the specification.

Dependent claim 20 recites:

The controller/driver according to claim 1, further comprising:

means for transferring said first bitmap data from said work memory to said display memory; and

means for displaying said second bitmap data output from said display memory on said display panel,

wherein a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel.

Support for *"means for transferring said first bitmap data from said work memory to said display memory"* may be found, for example, page 16, lines 8-12, and page 17, lines 4-16 of the specification. In particular, see memory controller 18 in the drawings, which controls the work memory 12 and the display memory 13.

Support for " *means for displaying said second bitmap data output from said display memory on said display panel*" may be found, for example, in Figure 3 of the drawings, and on page 18, line 27 to page 19, line 23 of the specification. In particular, see LCD 3 in the drawings, which displays second bitmap data.

Support for "*wherein a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel*" may be found, for example, on page 23, line 20 to page 24, line 7 of the specification.

7. Ground of Rejection to be Reviewed on Appeal

The ground of rejection to be reviewed on appeal is whether the Examiner erred in rejecting claims 1-3, 6-12 and 19 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,206,003 to Nose et al. ("Nose").

8. Argument

i) Claims 1-3, 6-11 and 19:

Claims 2-3, 6-11 and 19 depend ultimately from independent claim 1, and will be discussed herein with reference to claim 1.

Independent claim 1 recites:

a work memory;

a graphic engine converting externally received image data into first bitmap data, and storing said first bitmap data into said work memory;

a display memory receiving and storing second bitmap data developed from said first bitmap data stored in said work memory; *and*

a driver circuit which receives said second bitmap data from said display memory, and drives a display panel in response to said second bitmap data received from said display memory,

wherein said first bitmap data includes a plurality of line data each including a plurality of pixel data associated with respective pixels associated with a corresponding gate line of said display panel, and

wherein said data transfer of said first bitmap data from said work memory to said display memory is performed such that each of said plurality of line data is transferred at the same time in parallel from said work memory to said display memory. ***(emphasis added)***

The final Office Action asserts that the memory control circuit 6 of Nose corresponds to the claimed graphic engine. This assertion is incorrect. Figure 1 of Nose shows that the CPU 1 provides image data to a first display memory 7a and to an input port of a first selector 8. Figure 7 of Nose shows that the CPU 1 provides image data to an input port of a fourth selector 15 and to an input port of a first selector 8. The memory control circuit 6 of Nose only receives a memory control signal from the CPU 1. Because the memory control circuit 6 of Nose does not receive any such image data from the CPU 1 (or from any other element), the memory control circuit 6 of Nose cannot convert externally received image data, as recited in claim 1.

The memory control circuit 6 of Nose controls a first display memory 7a and a second display memory 7b by providing control signals to those display memories 7a, 7b, and consequently the memory control circuit 6 of Nose does not store any bitmap data into the

display memories 7a, 7b, as would be required for the features recited in claim 1. The final Office Action asserts that Nose's display memory 7b can operate as a work memory. Nose, however, does not meet the specific limitations recited in claim 1, because Nose's display memory 7b does not receive any bitmap data from its memory control circuit 6 (which the final Office Action asserts as corresponding to the claimed graphic engine), but rather it only receives control signals from that device.

The "Response to Arguments/Amendments/Remarks" section of the Final Action asserts that "The memory control circuit 6 must receive image data so that image data would be evenly divided into High and Low Order 4-bit corresponding to the correct First and Second Displays . . ." (Final Action at 10.) However, this assertion is incorrect. As Figure 7 of Nose illustrates, image data is provided from the CPU 1 directly to the inputs of the Fourth Selector 15 and the First Selector 8. The image data is not provided to the memory control circuit 6.

Page 11 of the final Office Action asserts that "The Examiner broadly interprets 'image data' comprises not only gradation data but also control and timing data for synchronization so that the desired images would have been produced sequentially and orderly." This assertion is contrary to the ordinary and customary meaning of the phrase "image data." Both Nose and the present invention distinguish between "image data" and "control signals". That is, control signals are provided by a CPU to a memory controller, and image data are not provided to the memory controller, as seen in Figure 1 of Nose. Note that a graphic engine 11 receives image data in Figure 1 of the drawings, and in which image data is provided to a Fourth Selector 15 and a First Selector 8 in Figure 7 of Nose. Thus, the broad interpretation of "image data" in the final Office Action to include control and timing data is improper.

Still further, the final Office Action incorrectly asserts that Nose's second selector 9 operates as a display memory. Nose's second selector 9, however, selects data from either a first display memory 7a or a second display memory 7b, and provides the selected data to a latch circuit 12. To assert that the data selected from the first and second display memories 7a, 7b by the second selector 9 "must be remained (or to be stored) in second selector 9 for a predetermined period of time" goes entirely against the standard and normal operation of a selector, which is to select one of a plurality of inputs for output, and not to store that data for

any pertinent length of time. Again, a selector 'selects' data for outputting, and a memory 'stores' data – these are entirely separate things.

Accordingly, presently pending independent claim 1, as well as its dependent claims 2-3, 6-11 and 19, are not anticipated by Nose.

ii) Claim 12:

Claim 12 depends ultimately from claim 1, and so the arguments provided above in Section i) apply equally as well to claim 12. Additionally, claim 12 is patentable for the following reasons.

Claim 12 recites:

a timing controller controlling said work memory, and said display memory, and said driver circuit,

wherein said driver circuit is connected to said second bit lines, and

wherein said ***timing controller is adapted*** *to deactivate said display memory* ***to allow said first bitmap data to be transmitted from said work memory to said driver circuit through said second bit lines***. (emphasis added).

In its rejection of claim 12, the final Office Action refers in part to Figure 5 of Nose, but the dashed lines provided in the top row of that figure show that no data is provided from the display memories 7a, 7b to the drive circuit, and thus no data is allowed to be transmitted to the drive circuit of Nose in that case.

Page 12 of the final Office Action, asserts that "the selector would not select (deactivated") since both Memory Partition Signal (Select 1) and Memory Read Select Signal (Select 2) are OFF) said display memory . . ." However, in Nose, when the Memory Partition Signal (Select 1) and the Memory Read Select Signal (Select 2) are OFF, then no bitmap data is outputted to Data Line Drive Circuit 13 (since nothing is output by the second selector and the third selector), and thus it does not meet the specific limitations recited in claim 12.

Accordingly, dependent claim 12 is patentable over the cited art of record for these additional reasons, beyond the reasons given above for its base claim 1.

iii) Claim 20:

Claim 20 depends from claim 1, and so the arguments provided above in Section i) apply equally as well to claim 20. Additionally, claim 20 is patentable for the following reasons.

Dependent claim 20 recites a transferring means and a displaying means, and it also recites that a first rate at which the first bitmap data is transferred from the work memory to the display memory is faster than a second rate at which the second bitmap data is output from the display memory for display on the display panel. In its rejection of claim 20, the final Office Action asserts that column 2, lines 1-10 of Patrick teaches the features recited in this claim. Applicants respectfully disagree.

Column 2, lines 1-10 of Patrick merely describes that the slower the rate of block transfers of data between memory locations, the slower the rate at which a computer system operates, and that block transfers of data between memory locations should be as fast as possible. This says nothing about having one block transfer rate between a first memory and a second memory and having a second block transfer rate (different from the first block transfer rate) between the second memory and another device (e.g., a display). Rather, Patrick would appear to teach having a same, fast transfer rate between all of the devices in his display system, which is totally different from the specific "different speed" features recited in claim 20.

Pages 12 and 13 of the final Office Action assert that column 2, lines 1-10 of Patrick does teach the use of two different speeds for transferring two different types of data, but this assertion reads much into Patrick that is simply not there. It appears, however, that the final Office Action is applying hindsight reconstruction of the claimed invention, by using features of Applicant's own specification and placing those features into a reference (Patrick) that does not teach or suggest such features. To the extent the Examiner is relying on column 2, lines 1-10 of Patrick, this portion of Patrick merely describes that "color, text and graphics" data should be transferred as fast as possible, to make the computer operate as fast as

possible. In any case, the use of hindsight reconstruction of the claimed invention is an improper basis for rejecting a claim.

Thus, dependent claim 20 patentably distinguishes over the cited art of record for these additional reasons, beyond the reasons given above for its base claim.

9. Conclusion

In view of above, Appellant requests that the rejection of the claims be reversed.

Respectfully submitted,

Date 9/20/2011 By _____

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10. EVIDENCE APPENDIX

None

11. RELATED PROCEEDINGS APPENDIX

None

12. CLAIMS APPENDIX

LIST OF THE CLAIMS ON APPEAL (WITH STATUS IDENTIFIERS)

1. (Previously Presented) A controller/driver comprising:

a work memory;

a graphic engine converting externally received image data into first bitmap data, and storing said first bitmap data into said work memory;

a display memory receiving and storing second bitmap data developed from said first bitmap data stored in said work memory; and

a driver circuit which receives said second bitmap data from said display memory, and drives a display panel in response to said second bitmap data received from said display memory,

wherein said first bitmap data includes a plurality of line data each including a plurality of pixel data associated with respective pixels associated with a corresponding gate line of said display panel, and

wherein said data transfer of said first bitmap data from said work memory to said display memory is performed such that each of said plurality of line data is transferred at the same time in parallel from said work memory to said display memory.

2. (Original) The controller/driver according to claim 1, wherein said image data is described in a vector format.

3. (Previously Presented) The controller/driver according to claim 1, wherein said image data includes compressed image data.

4. (Canceled).

5. (Canceled).

6. (Previously Presented) The controller/driver according to claim 1, further comprising:

a latch receiving said line data from said work memory, and temporally storing said received line data.

7. (Previously Presented) The controller/driver according to claim 1, further comprising:

a timing controller controlling said work memory, said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory is synchronous with readout of said second bitmap data from said display memory to said driver circuit; and

a memory controller connected to said second input port of said work memory, said memory controller receiving bit map data from a processor for storage in said display memory.

8. (Original) The controller/driver according to claim 7, wherein said data transfer of said first bitmap data from said work memory to said display memory is initiated in response to activation of a frame synchronization signal indicating to start displaying each image frame.

9. (Previously Presented) The controller/driver according to claim 7, wherein said timing controller controls said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory does not overrun said readout of said second bitmap data from said display memory to said driver circuit.

10. (Original) The controller/driver according to claim 1, wherein said work memory includes:

a plurality of first bit lines,

a plurality of first word lines, and

a plurality of first memory cells disposed at respective intersections of said first bit lines and first word lines to store therein said first bitmap data,

wherein said display memory includes:

a plurality of second bit lines,

a plurality of second word lines, and

a plurality of second memory cells disposed at respective intersections of said second bit lines and second word lines to store therein said second bitmap data,

wherein a number of said first bit lines is same as that of said second bit lines, and

wherein said first bit lines are connected to said second bit lines, respectively.

11. (Original) The controller/driver according to claim 10, wherein a number of said first word lines is identical to that of said second word lines.

12. (Previously Presented) The controller/driver according to claim 10, further comprising a timing controller controlling said work memory, and said display memory, and said driver circuit,

wherein said driver circuit is connected to said second bit lines, and

wherein said timing controller is adapted to deactivate said display memory to allow said first bitmap data to be transmitted from said work memory to said driver circuit through said second bit lines.

13. (Withdrawn) The controller/driver according to claim 12, wherein said timing controller is adapted to successively change portions of said first and second bitmap data stored in said work memory and said display memory to be transferred to said driver circuit.

14. (Withdrawn) The controller/driver according to claim 1, further comprising a processing circuit which processes said bitmap data received from said work memory to develop said bitmap data to be displayed and stores said developed bitmap data in said display memory.

15. (Withdrawn) The controller/driver according to claim 1, further comprising another processing circuit which processes said bitmap data stored in said display memory, and provides said processed bitmap data for said work memory.

16. (Withdrawn) A display device comprising:

a controller/driver; and

a first display panel including:

a plurality of first data lines, and

a plurality of first gate lines,

a second display panel including:

a plurality of second data lines respectively connected to said first data lines, and

a plurality of second gate lines,

wherein said controller driver includes:

a work memory comprising a plurality of first bit lines,

a graphic engine converting externally received image data into first bitmap data to store into said work memory,

a display memory storing a second bitmap data and comprising a plurality of second bit lines respectively connected to said first bit lines,

a data line driver driving said first data lines,

a first gate line driver driving said first gate lines,

a second gate line driver driving said second gate lines, and

a controller circuit controlling said work memory, said display memory, said data line driver, and said first and second gate line drivers,

wherein said controller circuit is adapted to deactivate said display memory to thereby allow said first bitmap data to be transmitted to said data line driver through said second bit lines, and to allow said second bitmap data to be transmitted from said display memory to said data line driver, and

wherein said controller circuit is adapted to control said first and second gate line drivers to allow said data line driver to drive said second data lines of said second display panel through said first data lines of said first display panel.

17. (Withdrawn) The display device according to claim 16, wherein said controller circuit is adapted said first and second gate line drivers to allow the same image to be displayed on said first and second display panels in response to one of said first and second bitmap data.

18. (Canceled).

19. (Previously Presented) The controller/driver according to claim 1, further comprising:

a latch receiving said first bitmap data from said work memory, and temporally storing said first bitmap data; and

a timing controller for controlling output of data from said latch,

wherein said display memory receives said first bitmap data output from said latch,

wherein said work memory and said display memory are operated at different times due to having said latch provided therebetween.

20. (Previously Presented) The controller/driver according to claim 1, further comprising:

means for transferring said first bitmap data from said work memory to said display memory; and

means for displaying said second bitmap data output from said display memory on said display panel,

wherein a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel.

21. (Withdrawn) The controller/driver according to claim 1, further comprising:

a graylevel converter interposed between the work memory and the display memory, the graylevel converter allowing a number of data bits corresponding to said first bitmap data stored in the work memory to be different from a number of data bits corresponding to said second bitmap data stored in the display memory.

22. (Withdrawn) The controller/driver according to claim 21, wherein the graylevel converter converts graylevels of the first bitmap data stored in the work memory so that an upper M bits of N bits associated with a particular color within each pixel data of the first bitmap data stored in the display memory is identical to the M bits of the associated pixel

data of the first bitmap data stored in the work memory, wherein M and N are integers, with M less than N.